Remarks

The above Amendments and these Remarks are in reply to the Office Action mailed January 29, 2003 ("Office Action") in patent application Serial No. 10/085,782.

Claims 1-2, 4, 6, 10-11, 15-16, 19-22, 24-25 and 28-29 have been amended.

In the Office Action, the Examiner objected to claims 10-11, 19-20 and 24-25, but indicated the claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant's attorney has rewritten claims 10-11, 19-20 and 24-25 in independent form. Accordingly, it is respectfully requested that the Examiner allow claims 10-11, 19-20 and 24-25.

The Examiner objected to the Abstract. The Applicant's attorney has amended the Abstract as suggested by the Examiner. Accordingly, it is respectfully requested that the Examiner withdraw the objection to the Abstract.

Claims 1-2, 6, 10, 16, 19 and 24 are objected to because of informalities. The Applicant's attorney has amended claims 1-2, 6, 10, 16, 19 and 24 as suggested by the Examiner. Other claims have likewise been amended to correct informalities. Accordingly, it is respectfully requested that the Examiner withdraw the objection to the claims.

Claims 1-9, 12-18 and 28-31 are rejected under 35 U.S.C. §102(b) as being anticipated by *Zerbe et al.* (U.S. Patent No. 6,111,445).

Claims 21-23 and 26-27 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Zerbe et al.* and Official Notice.

I. Rejection of Claims 1-9, 12-18 and 28-31 Under 35 U.S.C. §102(b)

Claims 1-9, 12-18 and 28-31 are rejected under 35 U.S.C. §102(b) as being anticipated by *Zerbe et al.*

Zerbe et al. teaches a phase interpolator with noise immunity. Abstract. The phase interpolator taught by *Zerbe et al.* includes numerous circuits as shown in Fig. 5. For example, the phase interpolator includes a voltage to current conversion circuit 2001, current mirroring 2002, current switches 2003 and load cell 2004. In particular, the outputs of current switches 2003 are input to load cell 2004.

Zerbe et al. is directed toward improving output signal jitter by rejecting noise on voltage supplies V_{dd} and V_{bb}. Col. 1, lines 55-67.

In direct contrast, embodiments of the present invention are directed toward improving a duty cycle of a clock signal as shown in Fig. 5. Improved duty cycle performance is obtained by improving current matching in a current mirror in an embodiment of the present invention. As described in the Background section of the present Application, current mismatching occurs when particular transistors are not operating in a saturation region of a particular circuit design. Thus, in an embodiment of the present invention, claimed circuit components and couplings that are not taught or suggested by *Zerbe et al.*, enable improved duty cycle performance.

A. Claims 1 and 15

In rejecting independent claims 1 and 15, the Examiner uses Fig. 18 in *Zerbe et al.* In particular, the Examiner stated Fig. 18 teaches:

> (a) a first node 2108 for providing a variable first voltage JX;
> (b) a second node 2109 for providing a variable second voltage JXB;
> (c) a first transistor 2806, coupled to the first node (at the drain), having a first gate for providing a first current (through transistor 2806) responsive to **a first control voltage (the voltage at the gate of 2806)** being applied to the first gate;
> (d) a second transistor 2802, coupled to the second node 2109 (at the drain), having a second gate for providing a second current responsive to **a second control voltage being applied to the second gate**;..... (Emphasis added.)

However, claims 1 and 15 call for "a first transistor" and "a second transistor" "capable to provide a first current" and "a second current responsive to a second control voltage" and "a first

control voltage." The first and second control voltages are provided by "a first control circuit" and "a second control circuit", not from the claimed "a first node" and "a second node." *Zerbe et al.* teaches a circuit in which node 2108 is connected to the gate of transistor 2802 and node 2109 is connected to the gate of transistor 2806. *Zerbe et al.* also teaches applying voltage JX at "a first node" (2108) **and** the gate of transistor 2802, and voltage JXB at "a second node" (2109) **and** the gate of transistor 2806. In sum, the Examiner is using the voltage JX and JXB at node 2108 and 2109 to be **both** the "first variable voltage" and "second variable voltage" as well as the "first control voltage" and "second control voltage" which is distinctly claimed as being provided by "a first control circuit" and "a second control circuit."

B. Claim 2

Claim 2 depends from independent claim 1 and therefore is patentable for at least the same reasons stated above.

C. Claim 3

Claim 3 depends from independent claim 1 and therefore is patentable for at least the same reasons stated above.

Further, claim 3 calls for "the first and second transistors operate in a saturation region." In rejecting claim 3, the Examiner stated

> ...[S]ince the Zerbe's first and second transistors have all the connections and configurations as discussed herein above, the Zerbe's first and second transistors must be assumed to operate in saturation region also. Office Action, page 5.

As described above, *Zerbe et al.* does not teach or suggest "all the connections and configurations" of claim 1; thus, *Zerbe et al.'s* first and second transistors cannot be assumed to operate in a saturation region.

D. Claims 4, 5, 7 and 9

Claims 4, 5, 7 and 9 ultimately depend from independent claim 1 and therefore are at least patentable for the same reasons stated above.

E. Claims 6 and 8

Claim 6 depends from independent claim 1 and therefore is at least patentable for the same reasons stated above.

Also, claim 6 calls for a further limitation that "the first variable voltage and the second variable voltage are obtained from a clock signal."

The Examiner states that the limitation is met because "nodes 2108 and 2109 can receive any signal." However, the Examiner has not cited a specific teaching of *Zerbe et al.* for this proposition. *Zerbe et al.* does not teach by way of Fig. 18 a circuit that can receive any input. *Zerbe et al.* teaches a very specific interface for the circuit shown in Fig. 18, in particular Fig. 18 teaches an embodiment of a load cell 2004 shown in Fig. 5. The inputs to load cell 2004, voltages JX and JXB, are obtained from current switches 2003.

Claim 8 calls for "first current, the second current, the third current and fourth current are used to provide a duty cycle correction signal."

As with claim 6, the Examiner has not provided specific teachings of *Zerbe et al.* for this proposition. *Zerbe et al.* teaches a circuit in Fig. 18 that has outputs to a phase comparator (shown in Fig. 5) and the Examiner has not identified where *Zerbe et al.* teaches using these outputs "to provide a duty cycle correction signal."

F. Claims 28-31

Independent claim 28 calls for a specific method according to an embodiment of the present invention.

The Examiner rejected claim 28 stating:

> ...[T]his claim is merely a method to operate the circuit having elements and connections discussed in claim 1 above, since Zerbe teaches the circuit, he inherently teaches the recited claim.

First, as described above, the circuit shown in Fig. 18 does not teach claim 1; therefore, the method to operate the circuit is not inherent.

Second, the Examiner has not shown where *Zerbe et al.* teaches "obtaining a clock signal" and "applying a first voltage from the clock signal to a first transistor ...." as required by the first two steps of claim 28.

Claims 29-31 ultimately depend from claim 28 and are there for patentable for at least the same reasons described above.

Further, claim 31, like claim 8, calls for an additional step of using currents "to provide a duty cycle correction signal" that is clearly not taught or suggested by *Zerbe et al.*

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of Claims 1-9, 12-18 and 28-31 under 35 U.S.C. §102(b) as being anticipated by *Zerbe et al.*

II. Rejection of Claims 21-23 and 26-27 Under 35 U.S.C. §103(a)

Claims 21-23 and 26-27 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Zerbe et al.* and Official Notice.

In rejecting claims 21-23 and 26-27, the Examiner combined the teachings of a *Zerbe et al.* load cell shown in fig. 18 and Official Notice (a memory system including a receive and transmit circuit is well known). The Examiner stated:

> The motivation and/or suggestion for doing so would have been obvious since by incorporating the Zerbe's interpolator circuit, noise immunity could be improved. Office Action, page 10.

However, *Zerbe et al.* teaches multiple load cell 2004 embodiments. The Examiner has used one load cell embodiment shown in Fig. 18 in rejecting the claims and ignored alternate load cell embodiments. The Examiner has not provided any reason or motivation why one of ordinary skill in the art would combine this particular load cell teaching instead of other embodiments or teachings of the cited art. *Zerbe et al.* teaches a current mirroring circuit 2002 that is directed toward matching currents; yet, the Examiner used the teachings of Fig. 18 rather than the teaching of current mirroring circuit 2002. In sum, the Examiner is using the present Application and impermissible hindsight in picking and choosing the teachings of *Zerbe et al.* to combine with Official Notice.

A. Claims 21-23 and 26

Independent claim 21, like claim 1, calls for a receive circuit that has a similarly included claimed circuit and is therefore patentable for at least the same reasons described above in regard to claim 1.

Claims 22-23 and 26, depend from claim 21, and are patentable for at least the same reasons.

Claim 27 calls for "the receive circuit is a circuit used for improving a clock signal."

In rejecting claim 27, the Examiner stated, "since the Zerbe circuit is for improving noise immunity, the recited limitation is met." The Applicant's attorney respectfully disagrees. Just because *Zerbe et al.* teaches a circuit that provides "noise immunity," *Zerbe et al.* does not necessarily teach a circuit that improves a clock signal. As described in the Background in the present Application, current mismatch due to transistor channel length effects and voltages used in a specific circuit design affect a clock signal. Specification, pages 2-3.

Accordingly, it is respectfully requested that the Examiner withdraw the rejection of Claims 21-23 and 26-27 under 35 U.S.C. §103(a) as being unpatentable over *Zerbe et al.*

III. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-31 is respectfully requested.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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